**San Jose State University**

**Department of Computer Engineering**

**CMPE 140 Lab Report**

**Lab 5 Report**

**Title** Processor Design (1): Design Code Review and Functional Verification

**Semester** \_\_\_\_\_\_\_\_\_\_\_\_ **Date** \_\_\_\_\_\_\_\_\_\_\_\_\_\_

**by**

**Name** \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ **SID** \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

*(typed) (typed)*

**Name** \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ **SID** \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

*(typed) (typed)*

**Lab Checkup Record**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Week** | **Performed**  **By**  **(signature)** | **Checked**  **By**  **(signature)** | **Tasks**  **Successfully**  **Completed\*** | **Tasks**  **Partially**  **Completed\*** | **Tasks Failed**  **or Not**  **Performed\*** |
| **1** |  |  |  |  |  |

**\* Detailed descriptions must be given in the report.**